33rd ICMTS

2020 IEEE International Conference on Microelectronic Test Structures

May 4–17, 2020

Sponsored by:
The IEEE Electron Devices Society

THE UNIVERSITY *of* EDINBURGH
School of Engineering

Contents

WELCOME LETTER

Dear Colleagues,

On behalf of the organising committee of the 2020 IEEE International Conference on Microelectronic Test Structures I would like to thank you for your interest in the conference. Obviously we are very sad that the meeting will not go ahead as planned in the wonderful city of Edinburgh but we hope you will enjoy the experience of the virtual conference. This is the 33rd ICMTS conference and it would have been the third time in Edinburgh. The conference is being run in co-operation with the University of Edinburgh and is co-sponsored by the IEEE Electron Devices Society. We have had invaluable support from the EDS, as well as the IEEE Meetings and Conferences, and Digital Events Teams in organising the virtual event. I would also like to thank the ICMTS Steering Committee and our local organising team in the School of Engineering for their help, it would not have been possible without them.

I have been a regular attendee at ICMTS since Göteborg in 1999 when I was a first year PhD student and a very nervous speaker. This year one of the papers is authored by a recent PhD graduate of mine and I am extremely honoured to act as your conference chair. Over the last three decades the conference has provided an invaluable forum for designers and users of test structures while the microelectronics industry has matured and changed. The biggest change in the conference content is probably the increasing number of papers focussing on the fabrication of micro and nano-systems including micromechanical systems, novel sensors etc. (More that Moore technology) alongside the more traditional topics concerning advanced microelectronic processes. Most recently we've seen increasing numbers of papers looking non-volatile memories, silicon based photonics and packaging. The ability of ICMTS delegates to apply their expertise in test and measurement to new technologies and applications is extremely exciting to see and bodes well for the future of the conference.

While I am very sad to be unable to welcome you to Edinburgh in person this year I look forward to your participation in the ICMTS 2020 virtual meeting and I hope to see many of you again in a more normal situation at the next conference.

Sincerely,

Stewart Smith,
General Chair.

GENERAL INFORMATION

Conference Information

The 2020 International Conference on Microelectronic Test Structures is financially sponsored by the IEEE Electron Devices Society. The conference is also being supported by the School of Engineering at the University of Edinburgh. The purpose is to bring together designers and users of test structures to discuss recent developments and future directions.

Website and Email Contacts

ICMTS Website:
http//:www.icmts.net/
Email Contact:
icmts@ed.ac.uk

Presentations

The official language of the conference is English. This year all presentations will be oral and the time allowed for each speaker is 15 minutes. Extended invited presentations will be around 30 minutes.

Presentation recordings will be available to view on the virtual conference website from the 4th of May 2020 until the 17th of May. Registration for the conference will allow access to the recorded presentations and the ability to ask questions of the authors. Sessions will be moderated by members of the ICMTS technical committee who will direct answers back to the conference website.

Best Paper Award

The best paper will be announced shortly after the end of the conference and the award will be made at ICMTS 2021.

Conference Proceedings

The conference proceedings will be published in electronic format and as an optional printed proceedings. PDF files of all accepted papers will be available to those who have registered. Printed copies of the proceedings may be ordered as an optional extra when registering for the conference for £20 per copy.

Conference Registration

Registration Fees

Virtual Conference

	Member*	Non Member	Student**
Technical Sessions	£125	£150	£100/£110

* Must be a member of the IEEE

** Lower prices for student members of IEEE

Payment of Registration Fees

Payment should be made using the University of Edinburgh's on-line payments system:

ePay Website

The conference epay page can also be accessed via a link on the ICMTS website:

http://www.icmts.net/

Registering for the conference will allow you to add the option of a printed proceedings.

TUTORIALS

Unfortunately we have made the difficult decision to cancel the tutorials this year. We hope that some of the exciting and informative lectures planned for this year's tutorial will be able to move to the conference in 2021.

EQUIPMENT EXHIBITION

The following test equipment companies have contributed to the sponsorship of the conference. We would like to thank them for their continued support of ICMTS 2020 at this difficult time. Please go to the Exhibitor Presentation Session to view their video contributions.

- Keysight Technologies
- MPI Corporation
- ProPlus Design Solutions Inc.
- Lambda Photometrics Ltd.
- Celadon Systems Inc.

TECHNICAL PROGRAM

Additional Session Links

Welcome Session
ICMTS 2021 Announcement
Exhibitor Presentations
Special Thanks from Steering Committee
Closing Remarks

INVITED SESSION

Session Chair: Stewart Smith, *School of Engineering, The University of Edinburgh, Scotland*

Invited Presentations

Keynote 1 – History and future of measurement instruments for semiconductor parameter analysis
Satoshi Habu
Keysight, Japan
In 1982, the first SMU based measurement instrument was introduced. It changed style of semiconductor researches and took researches to another level. The introduction was not consequence of a chance event, but inevitable consequence to meet with demands at the time. This talk tries to review history of demands before and after the first introduction and evolutions of measurement instruments for the demands. Expected future trends of instruments will be provided based on the reviewed history.

Keynote 2 – Experimental Set-Up For Novel Energy Efficient Charge-based Resistive RAM (RRAM) Switching
Paola Trotti, S. Oukassi, G. Pillonet, G. Molas, E. Nowak
CEA Leti, France
This work explores a new method to reduce the energy consumption during the writing of process-spread resistive-based memories (RRAM), based on setting an initial electrical charge into a writing capacitor rather than applying constant voltage over a fixed time. By connecting a charged capacitor (constant charge source, CQS) to a RRAM device, we benefit of a lower energy requirement for setting the memory cells, for a given success rate. We derive a statistical RRAM compact model from experimental data, and benchmark our proposed writing procedure with respect to the constant voltage source (CVS) approach. Finally, we give experimental proof of concept by realization of a circuit interface that integrates the CQS protocol, connected to a RRAM load. Results support the fact that setting the initial charge is a better choice to control efficiently the variability of the filamentary process in RRAM.

SESSION 1: Advanced Measurement Techniques

Session Chair: Bill Verzi, *Verzitest, Austin, TX, USA*

Session 1 Presentations

1.1 – Process Variation Estimation using An IDDQ Test and FlipFlop Retention Characteristics

Shinichi Nishizawa[1] and Kazuhito Ito[1]
[1]*Faculty of Engineering, Fukuoka University;* [2]*Graduate School of Science and Engineering, Saitama University, Japan*

Extraction method of process variation is proposed. Process monitor circuits are widely used for the extraction of process variation, however adding special purpose circuit increase the silicon area. Usually, silicon chips are tested electrically and functionally after the fabrication. IDDQ test is an electrical test which measures leakage current and find the fault in the target chip. Scan-test is a functional test which inputs and measures the internal signal vector using scan- flip-flop. We propose to an extraction method of process variation utilizing IDDQ test and retention characteristics of scan-flip-flop. This method enables process variation extraction without any extra process monitor circuit. Test structures are implemented into silicon chips and result shows global variation shift is extracted as threshold voltage shift.

1.2 – Calibration of CBCM Measurement Hardware

Brad Smith[1], Emmanuel Onyegam[1], Donald Hall[1], and Bill Verzi[2]
[1]*NXP Semiconductors, Austin, Texas, USA;* [2]*Verzitest, Austin, Texas, USA*

CBCM measurements require precise measurement of AC currents. This work describes a test structure that was used to demonstrate capability of test hardware to be used for that measurement. A series of inverters was used to create periodic spikes of current of three magnitudes and at a wide range of frequencies. Current measurements using a Keysight 4072 tester were completely linear with frequency across a four-decade frequency range, and for average currents as low as 530 pA. This technique could be used to validate the limits any test hardware prior to designing an AC circuit.

SESSION 2: Parametric Tests

Session Chair: Christopher Hess, *PDF Solutions, USA*

Session 2 Presentations

2.1 – Standardization of Specific Contact Resistivity Measurements using Transmission Line Method (TLM)

Sidhant Grover[1], Shubham Sahu[1], Peng Zhang[2] and Santosh K. Kurinec[1]
[1]*Department of Electrical and Microelectronic Engineering, Rochester Institute of Technology, NY, USA;* [2]*Department of*

Electrical and Computer Engineering, Michigan State University, MI, USA

This study investigates the effect of TLM dimensions on the extracted values of specific contact resistivity ρ_c. It is observed that the extracted ρ_c depends on the TLM design, which varies for different applications. It is recommended that TLM dimensions be standardized for respective application used in structures, for example in ICs and solar cells.

2.2 – Automated Generation and Measurement of Parametric Test Structures

Paul Sullivan, Andreas Tsiamis, Stewart Smith, Anthony J. Walton and Jonathan G. Terry

School of Engineering, The University of Edinburgh, Scotland, UK

This paper reports the development of a process control chip compiler that automates the design of test chips for an optical direct write exposure tool (ML3 DMO). In addition to taking full advantage of inbuilt features of the DMO tool, the system also generates the software to characterise the specified test structures and this is interfaced to an automatic prober (Karl Suss PA 200) and a HP4062 rack of instrumentation. It uses open-source software (Python) and in contrast to previously reported parametric compilers this system is the first one specifically designed for an optical maskless lithography system targeted at rapid prototyping of microsystems.

2.3 – Characterization of parametric mismatch attributable to plastic chip encapsulation

Hans Tuinhout, Andrei Damian and Adrie Zegers-van Duijnhoven

NXP Semiconductors, the Netherlands

This paper discusses a test structure and associated high-precision characterization approach to study mechanical- stress-induced deterministic and random performance changes of semiconductor devices in plastic encapsulated chips. The results quantify effects of lead frame mounting, wire bonding and molding and demonstrate the positive effects of a stress buffer layer.

2.4 – Extraction of Ultra-Low Contact Resistivity by End-Resistance Method

Bing-Yue Tsui[1], Ya-Hsin Lee[1], Dong-Ying Wu[1], Yao-Jen Lee[2], and Mei-Yi Li[2]

[1] *Institute of Electronics, National Chiao-Tung University, Taiwan, R. O. C.;* [2] *Taiwan Semiconductor Research Center, Taiwan, R.O.C.*

The accuracy of extracting ultra-low contact resistivity (ρ_c) by the end-resistance method is evaluated. As the contact length (L_c) becomes smaller than the transfer length (L_t), the end-resistance (R_e) approaches the contact resistance (R_c), and the error decreases with the reduction of L_c and ρ_c. This end-resistance method is verified by self-aligned TLM test structure.

SESSION 3: Noise Measurements

Session Chair: Satoshi Habu, *Keysight Japan*

Session 3 Presentations

3.1 – Area-Efficient and Bias-Flexible Inline Monitoring Structure for Fast Characterization of RTN and Transistor Local Mismatch in Advanced Technologies

A. Jayakumar, N.Chan, L.Pirro, O. Zimmerhackl, M. Otto, T. Kleissner and J. Hoentschel

GLOBALFOUNDRIES Fab1 LLC & Co.KG, Wilschdorfer Landstrasse 101, 01109 Dresden, Saxony, Germany

An improved set of Scribe Line Monitors (SLMs) with high device densities have been designed for inline monitoring of Random Telegraph Noise (RTN) and transistor local mismatch. This infrastructure offers increased statistics from measurement on a single wafer with parallel Device Under Test (DUT) testing capability thereby having an efficient testing time. The characteri- zation results from engineering silicon are presented in this paper.

3.2 – Test Structures for Noise Reduction of Fully Depletion-Silicon on Insulator p-Type Tunneling FET Using Channel Orientation

Hyun-Dong Song, Hyeong-Sub Song, Sunil Babu Eadi, Hyun-Woong Choi, Ga-Won Lee, and Hi-Deok Lee

Department of Electronics Engineering, Chungnam National University

In this paper, the channel orientation of TFET is focused. The Proposed test pattern involves rotating TFET in the layout step to change the direction of the channel. As a result, the subthreshold slope and on-current are improved. Especially, low-frequency noise of devised pattern at 10 Hz reduced by about 100 times than normal TFET. The reason for improvement could be due to the distance between the silicon atoms increased, the Coulomb force, which affects the tunneling of the carrier, decreases.

3.3 – Increased Delay Variability due to Random Telegraph Noise under Dynamic Back-gate Tuning

Misaki Udo[1], Kensuke Murakami[2], A.K.M. Mahfuzul Islam[3] and Hidetoshi Onodera[2]

[1] *Undergraduate School of Electrical and Electronic Engineering, Kyoto University, Japan;* [2] *Graduate School of Informatics, Kyoto University, Japan;* [3] *Graduate School of Engineering, Kyoto University, Japan*

For the near- or sub-threshold region operation to achieve minimum energy, it is often ignored that dynamic tuning of voltage causes additional delay variability. In this paper, we raise a concern on the increased delay variability when dynamic tuning of back-gate voltage is employed. The mechanism of the increase of variability under dynamic tuning of supply voltage and back-gate voltage is explained. Using the measurement results, the impact of back-gate tuning on delay variability is demonstrated, which should be considered for reliable circuit operation.

SESSION 4: MEMS Device Characterisation

Session Chair: Anthony Walton *The University of Edinburgh, Scotland, UK*

Session 4 Presentations

4.1 – Automated Wafer-Level Characterisation of Electrochemical Test Structures for Wafer Scanning

I. Schmueser, L. Mackay, F. Moore, K. Doherty, J. P. Elliott, A.R. Mount, A. J. Walton, S. Smith, and J. G. Terry
The University of Edinburgh, Scotland, UK

This paper presents an automated system for the electrochemical characterisation of micro-scale test structures at the wafer level, with the objective to identify good wafers suitable for full characterisation and device packaging. The integration of the on-wafer characterisation enables a quality assessment of the devices prior to packaging ensuring the development of this technology minimises the packaging of faulty sensors. The prototype system integrates all the elements for automated on-wafer in-line characterisation of electrochemically based systems thereby confirming the suitability of this approach for implementation on commercial automated probers, which are generally available for parametric testing. The system's capabilities are demonstrated on a three-electrode cell design typically employed in electrochemical sensing applications.

4.2 – Verification and Induction Method for Low Frequency Response-based Failure Modes in Acoustic MEMS

Gergely Hantos and Marc Desmulliez
Heriot-Watt University, School of Engineering & Physical Sciences, Edinburgh, UK

In this paper we present a novel verification and induction method for low frequency response-based failure modes in MEMS microphones. Response of the device is captured before and after focus ion beam induced defect in the diaphragm of the microphone. The deviation in the response is correlated to analytical results.

4.3 – A Rapid, Reliable and Less-destructive On-chip Mass Measurement for 3D Composite Material Testing Microstructures

Gilgueng Hwang[1,2,3], Christophe David[3], Alisier Paris[3], Dominique Decanini[3], Ayako Mizushima[4], Yoshio Mita[1,2]
[1] *LIMMS-CNRS, Institute of Industrial Science, University of Tokyo, Japan;* [2] *Dept. of Electrical Engineering and Information Systems, The University of Tokyo, Japan;* [3] *C2N-CNRS, University Paris-Sud, France;* [4] *VLSI Design and Education Center, The University of Tokyo, Japan*

We have demonstrated a rapid, reliable and less-destructive on-chip mass measurement method. It is based on AFM pick-measure-place micromanipulation using Van der Waals attraction and the mass measurement by resonant frequency shift. The measurement sensitivity revealed to be 25 Hz/pg and it could be promising to characterize MEMS with complex geometries and composite materials.

4.4 – Test structure and measurement system for characterising the electrochemical performance of nanoelectrode structures

I. Schmueser[1], E.O. Blair[1,2], Z. Isiksacan[1,3], Y. Li[1,4], D.K. Corrigan[1,2], A.A. Stokes[1], J.G. Terry[1], A.R. Mount[1] and A.J. Walton[1]

[1] *The University of Edinburgh, Scotland, UK;* [2] *University of Strathclyde, UK;* [3] *Northumbria University, UK;* [4] *Bilkent University, Turkey*

This paper presents a complete test structure and characterisation system for the evaluation of nanoelectrode technology, which integrates microfabricated nanoelectrodes, 3D printing and surface tension-confined microfluidics. This system exploits the inherent analytical advantages of nanoelectrodes that enables their operation with small volume samples, which has potential applications for on-wafer measurements.

SESSION 5: Materials Characterization

Session Chair: Hans Tuinhout, *NXP Semiconductors, The Netherlands*

Session 5 Presentations

5.1 – Multiscale modeling of charge transport properties and defect characterization of high-κ bilayer CeO_2/La_2O_3

Behnood Dianat, Paolo La Torraca, Yuri Ricci, Luca Larcher
University of Modena and Reggio Emilia, Italy

Presence of defects in high-κ gate dielectric materials such as cerium oxide and lanthanum oxide affects electrical properties of these materials. Hence, Intrinsic and defect characteristics of CeO_2 and La_2O_3 were investigated. In this work a comprehensive charge transport model was used to study carrier conduction through the device. After defect characterization, it was found that neutral vacancies (V_0) has the most contribution to electron/hole conduction. Trap energy levels for La_2O_3 and CeO_2 are 2.1 and 1.7 eV below conduction-band respectively which agrees with other reports. Carrier conduction through traps are perfectly explained by trap-assisted-transport mechanism.

5.2 – Electrical and optical localisation of leakage current and breakdown point in SiOC:H low-κ dielectrics

Matthias Vidal-Dhô[1,2], Quentin Hubert[1], Patrice Gonon[2], Bernard Pelissier[2], Philippe Lentrein[1], Patrice Ray[1], Jean-Michel Moragues[1], Pascal Fornara[1]

[1] *STMicroelectronics Rousset, France* [2] *LTM CNRS, Grenoble, France*

This paper presents a novel methodology to observe the leakage current origin in SiOC:H low-κ intermetallic dielectric (IMD) as well as a method to localise electrically the breakdown point in usual comb/serpentine/comb structures. Our results indicate that high leakage current is a consequence of a global moisture-induced SiOC:H dielectric modification and demonstrate that EMMI observations of such leakage current is possible. Besides,

we have disclosed and validated a fast electrical breakdown localisation method fully compatible with automated test steps such as Parametric Test to track eventual weaknesses in reliability structures for instance.

5.4 – OxRAM BER scaling trends on 4kb mixed-diameter test vehicle

J. Sandrini, C. Cagli, L. Grenoiullet, N. Castellani, V. Meli, F. Gaillard

CEA-LETI, Minatec Campus, Grenoble France

We show a 4kb OxRAM test structure which includes devices of diameters ranging from 30 nm to 170 nm. This matrix allows to evaluate the impact of scaling over several performance metrics. We show that dual-bit cells allow a 10× BER reduction compared to single ones at the same area.

5.5 – Doughnut Test Structure to Evaluate ZnO/Si Heterostructure to Improve Efficiency of PbS QD/ZnO/Si Hybrid Infrared Photodiode

Norihiro Miyazawa[1], Naoto Usami[1], Haibin Wang[2], Takaya Kubo[2], Hiroshi Segawa[2], Yoshio Mita[1,3] and Akio Higo[3]

[1]*Department of Electrical Engineering and Information Systems;* [2]*Research Center for Advanced Science and Technology;* [3]*Systems Design Lab, School of Engineering, The University of Tokyo, Japan.*

Hybrid infrared-sensitive optoelectronic device on silicon-based LSI is under investigation. In the last ICMTS, we have reported that heterojunction of PbS colloidal quantum dots and ZnO nanowires over ITO electrode gave very high External Quantum Efficiency (EQE over 30% for 1300nm), but PbS-ZnO on our n-type Si substrate gave very low EQE (0.6%). To locate the cause of the low device efficiency, we applied doughnut-shape test structure to ZnO/Si interface. As a result, we found that ZnO/Si junction behaved like current-limitting diode. Accordingly, the usefulness of employed test structure for investigating the heterojunction was confirmed.

SESSION 6: MEMS Process Characterization

Session Chair: Brad Smith, *NXP Semiconductors, USA*

Session 6 Presentations

6.1 – A nondestructive analysis method for the releasing process of thermal sensors

Chao Liu[1,2], Jianyu Fu[1,2,3], Ying Hou[1,2,3], Ruiwen Liu[1], Qiong Zhou[1,2,3], Dapeng Chen[1,2,3]

[1]*Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China;* [2]*University of the Chinese Academy of Sciences, Beijing, China;* [3]*Wuxi Innovation Center for Internet of Things, Jiangsu Wuxi, China*

Releasing process is a crucial technology to fabricate the suspended structure but easy to generate insufficient release and over release defects. We proposed a nondestructive analysis method to detect the releasing defects by analyzing their thermal parameters of thermal sensors. The analysis results are

consistent with the SEM results for the different releasing morphologies.

6.2 – Drop-in test structure chip to visualize residual stress of Cu supercritical-fluids-deposition (SCFD)
Naoto Usami[1], Etsuko Ota[2], Akio Higo[2], Takeshi Momose[3] and Yoshio Mita[1,2]
[1]*Department of Electrical Engineering and Information Systems (EEIS), The University of Tokyo, Japan;* [2]*Systems Design Lab (d.lab), The University of Tokyo, Japan;* [3]*Department of Materials Engineering, The University of Tokyo, Japan*
We propose a drop-in test structure chip to evaluate residual stress in Cu film induced during supercritical fluid deposition (SCFD) process. Despite its importance, classical stress evaluation methods such as wafer curvature radius measurement is difficult to be applied to SCFD film because the sample chip size is small. We propose to "drop-in" a test chip on with free-standing MEMS test structure. It is thereby possible to extract information on reliability and reproductivity of SCFD without destroying the sample chip. A selective deposition on microcantilevers is utilized for stress visualization and revealed tensile-stress under the tested condition.

6.3 – Microheater isolation characterisation to aid the optimisation of a MEMS Leidenfrost engine Anthony Buchoux[1], Prashant Agrawal[2], Gary G. Wells[2], Rodrigo Ledesma-Aguilar[2], Anthony J. Walton[3], Jonathan G. Terry[3], Glen McHale[2], Khellil Sefiane[1], and Adam A. Stokes[3]
[1]*School of Engineering, Institute for Multiscale Thermofluids, The University of Edinburgh, Edinburgh, UK;* [2]*Smart Materials & Surfaces Laboratory, Faculty of Engineering & Environment, Northumbria University, Newcastle upon Tyne, UK;* [3]*School of Engineering, Institute for Integrated Micro and Nano Systems, The University of Edinburgh, Edinburgh, UK*
This paper reports on the implementation of test structures to characterise the design of a microheater that will allow localised heating to power Leidenfrost micro-engines. These structures involve etching trenches in a silicon substrate to enable characterisation of their effect on heat transfer. Initial results indicate that a trench just 218 μm deep (less than half-way through the silicon substrate), results in the temperature in a region outside of the microheater device area being reduced by 3.6 ± 0.2°C after being powered for 2 mins.

6.4 – Test structure for measuring etch selectivity in vapour etch processes
Markus Rondé, Anthony J. Walton, Jonathan G. Terry
School of Engineering, Institute of Integrated Micro and Nano Systems, University of Edinburgh, UK
Etch selectivity between layers is an extremely important concern in the fabrication of microelectronics and microsystems. This is particularly true in the case of vapour etching methods used to release free standing structures through the selective etching of sacrificial layers. Commonly used structural materials have been reported to be largely inert when exposed to

a given vapour etchant, indicating high selectivity when measured against typical sacrificial layers. However, there is growing evidence that these structural layers are actually etched at an enhanced rate if they are located in the proximity of the sacrificial layer being removed. Hence, removal rates given in the literature that have resulted from measurements of layers that have been etched in isolation can no longer be trusted to characterise critical etch processes in device fabrication. In this paper, a test structure is reported that enables a far more accurate determination of the etch selectivity between sacrificial and structural materials.

SESSION 7: RF Device Characterization

Sesssion Chair: Francesco Driussi, *Università di Udine, Italy*

Session 7 Presentations

7.1 – Novel Statistical Modeling and Parameter Extraction Methodology of Cutoff Frequency for RF-MOSFETs
Chika Tanaka, Yasuhiko Iguchi, Atsushi Sueoka, and Sadayuki Yoshitomi
Memory Division, Kioxia Corporation, Yokohama, Japan
The cutoff frequency (f_T) fluctuation in RF-MOSFET had been investigated. Detailed analysis for capacitance fluctuation as well as the extraction of intrinsic parameter were performed. The global statistical f_T model was successfully developed in terms of capacitance fluctuation, considering intrinsic and extrinsic components separately and identifying the major variability sources.

7.2 – Influence of series resistance on the experimental extraction of FinFET noise parameters
Angeliki Tataridou*, Gerard Ghibaudo, Christoforos Theodorou
IMEP-LAHC, Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP Grenoble, France
In this paper we demonstrate for the first time how the series resistance of a FinFET device can lead to an incorrect extraction of noise parameters, especially concerning the mobility fluctuations, correlated to the carrier number fluctuations. We also present an original method for suppressing this effect, by taking advantage of the series resistance immune Y-function.

7.3 – Comparison of nMOSFET Structures for Millimeter-Wave Frequencies in 0.18μm CMOS technology
Toyoyuki Hagiwara, Natsu Yamaki, Kyoya Takano, Yohtaro Umeda
Department of Electrical Engineering, Faculty of Science and Technology, Tokyo University of Science Chiba, Japan
We present two nMOSFET structures (A: compact-type B: round-table-type) with the high maximum oscillation frequency (f_{max}) in 1P5M 0.18-μm CMOS technology for millimeter-wave applications. By reducing their parasitics, we achieve the f_{max} of 95 GHz, which is approximately 2 times compared to that of the conventional structure previously reported.

7.4 – Investigation of Test Structures for the Characterization of Very Fast Electro Static Discharge Events
Matt Lauderdale, Emmanuel Onyegam, Scott Ruth, Brad Smith and Alex Gerdemann
NXP Semiconductors, Austin, Texas, USA

New wafer technologies and chip design requirements are increasingly susceptible to damage from smaller Electro Static Discharge events (ESD). A method is needed to evaluate ESD risk posed by processing equipment and the effectiveness of proposed upgrades. This paper proposes and investigates a packaged test structure designed to measure ESD events. The test chip would run in the place of production parts during equipment and package level process evaluations. A design is proposed, developed and preliminary test results demonstrating feasibility are shown.

7.5 – Application of Broadband RF Metrology to Integrated Circuit Interconnect Reliability Analyses: Monitoring Copper Interconnect Corrosion in 3D-ICs
Papa K. Amoah, Jesus Perez, and Yaw S. Obeng
Nanoscale Device Characterization Division, Physical Measurement Laboratory, National Institute of Standards and Technology 100 Bureau Drive, Gaithersburg, MD, USA

In this talk, we will describe the development, and application, of a suite of high-frequency electromagnetic waves (RF) based techniques to probe material and structural changes in copper interconnects in TSV enabled 3-D integrated circuits during high-temperature storage. We discuss how RF insertion loss (S21) based-techniques have been used to study the oxidation of copper interconnects in 3D-ICs. We will compare the insertion loss results to those from DC measurements and discuss the advantages of the former technique over the latter. Using electrodynamic simulations, we will also discuss the partitioning of microwave signal loss in corroded copper interconnects, and the significance of the roughness at the air-copper oxide interface.

SESSION 8: MOSFET characterization

Session Chair: Jonathan Terry, *The University of Edinburgh, Scotland, UK*

Session 8 Presentations

8.1 – Anomalous scaling of parasitic capacitance in FETs with a high-K channel material
A.E.M. Smink, M.J. de Jong, H. Hilgenkamp, W.G. van der Wiel, and J. Schmitz
MESA+ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands

We investigate FET operation in devices of which the channel consists of a 2-dimensional electron system at the surface of a high-K channel material, $SrTiO_3$ ($K = 300$). Our devices have low gate leakage and are the first of their kind with a sub-nm equivalent oxide thickness, which can only be properly

determined after subtracting a parasitic capacitance that has an unusual 1/3-power dependence on the device length and width.

8.2 – Comparison of Extraction Methods for Threshold Voltage Shift in NBTI Characterization

Yu-Hsing Cheng, Michael Cook, Chris Kendrick
Corporate Research and Development, ON Semiconductor 1900 South County Trail, East Greenwich, RI 02818, USA

Extraction methods for threshold voltage shift in NBTI characterization were compared and evaluated for 3.3 V PMOS devices in a 0.18 μm process. The methodology in this work provides validation method of single ID measurement for fast determination of V_T shift in NBTI to check if they are applicable for the specific process.

8.3 – Integrated Variability Measurements of 28nm FDSOI MOSFETs down to 4.2 K for Cryogenic CMOS Applications

B. Cardoso Paz[1], L. Le Guevel[1], M. Cassé[1], G. Billiot[1], G. Pillonnet[1], A.G.M. Jansen[2], S. Haendler[3], A. Juge[3], E. Vincent[3], P. Galy[3], G. Ghibaudo[4], M. Vinet[1], S. de Franceschi[2], T. Meunier[5] and F. Gaillard[1]
[1]*CEA-Leti, Université Grenoble Alpes, MINATEC Campus, 38054 Grenoble, France;* [2]*Université Grenoble Alpes, CEA-IRIG, Grenoble, France;* [3]*STMicroelectronics, 38920 Crolles, France;* [4]*IMEP-LAHC, CNRS, Université Grenoble Alpes, MINATEC Campus, 38016 Grenoble, France;* [5]*Université Grenoble Alpes, Institut Néel, Grenoble, France*

Mismatch performance of 28nm FDSOI technology is electrically characterized at low temperatures using integrated on-chip addressing for a matrix of transistors. The first statistical results ever published on FDSOI variability at 4.2K provide valuable information for future compact transistor modeling in cryogenic circuit design.

8.4 – Generalized Constant Current Method in Weak and Moderate Inversion for Determining MOSFET Threshold Voltage

Matthias Bucher, Nikolaos Makris and Loukas Chevas
School of Electrical and Computer Engineering Technical University of Crete, Greece

A novel methodology for the extraction of threshold voltage and substrate effect parameters of MOSFETs biased in weak and moderate inversion is presented. This generalized constant-current method (GCCM) exploits the charge-based model of MOSFETs, and covers effects of edge conduction or subthreshold hump in MOSFETs using Shallow Trench Isolation (STI).

SESSION 9: Optoelectronic Device Characterization

Sesssion Chair: Carlo Cagli, *CEA Leti, France*

Session 9 Presentations

9.1 – Comparison of cut-back method and optical backscatter reflectometry for wafer level waveguide characterization

Anna Pęczek[1], Christian Mai[2], Georg Winzer[2] and Lars Zimmermann[2,3]

[1]*IHP Solutions GmbH, Frankfurt (Oder), Germany;* [2]*IHP, Frankfurt (Oder), Germany;* [3]*Technische Universität Berlin, Berlin, Germany*

The optimum optical characterization method suitable for wafer level waveguide testing is an important issue for silicon photonic methodology. In this paper we focus on comparing the two most widespread measurement techniques: cut-back and optical backscatter reflectometry. Wafer level test results are compared for different types of waveguides.

9.2 – Diode design for studying material defect distributions with avalanche-mode light emission

M. Krakers[1], T. Knezevic[1,2], K.M. Batenburg[1], X. Liu[1], L.K. Nanver[1]

[1]*MESA+ Institute, Faculty of EEMCS, University of Twente, Enschede, The Netherlands;* [2]*Micro and Nano Electronics Laboratory, Faculty of Electrical Engineering and Computing, University of Zagreb, Croatia*

Avalanche-mode visual light emission in Si diodes is shown to be useful for rapid assessment of the origin of non-ideal currents. In the test structure design it was important to consider the breakdown- voltage distribution, diode size and contact positioning to obtain light-spot appearances at positions related to bulk defect distributions.

9.3 – Experimental and simulation analysis of carrier lifetimes in GaAs/AlGaAs Avalanche Photo–Diodes

F. Driussi[1], A. Pilotto[1], D. De Belli[1], M. Antonelli[3], F. Arfelli[4,6], G. Biasiol[5], G. Cautero[3,6], R. H. Menk[3,6], C. Nichetti[3,4], L. Selmi[2], T. Steinhartova[4,6], P. Palestri[1]

[1]*DPIA, Università degli Studi di Udine, Udine, Italy;* [2]*Università di Modena e Reggio Emilia, Modena, Italy;* [3]*Elettra–Sincrotrone Trieste S.C.p.A, Trieste, Italy;* [4]*Università di Trieste, Department of Physics, Trieste, Italy;* [5]*IOM CNR, Laboratorio TASC, Trieste, Italy;* [6]*Istituto Nazionale di Fisica Nucleare, Trieste, Italy*

Extensive experimental characterization and TCAD simulation analysis have been used to study the dark current in Avalanche Photo–Diodes (APDs). The comparison between the temperature dependence of measurements and simulations points out that SRH generation/recombination is responsible for the observed dark current. After the extraction of the carrier lifetimes in the GaAs layers, they have been used to predict the APD collection efficiency of the photo–generated currents, that is of about 55% under realistic operation conditions.

9.4 – Test Setup Optimization and Automation for Accurate Silicon Photonic Wafer Acceptance Production Tests

Choon Beng Sia[1], Tiong Leh Yap[2], Ashesh Sasidharan[2], Jun Hao Tan[2], Robin Chen[2], Jacobus Leo[2], Soon Leng Tan[2] and Guo Chang Man[2]

[1] *FormFactor Inc.;* [2] *GlobalFoundries Singapore Pte Ltd*

Implementing energy-efficient optical transceivers with silicon photonics (SiPh) technology for hyperscale data centers will help alleviate the increasing energy demand, expected to be 20% of Earth's total energy output by 2030. To facilitate SiPh wafer acceptance tests, this paper proposes methods to optimize and implement a fully automatic SiPh wafer test architecture.

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WS	1986	Feb 17–18	Long Beach	USA
1	1988	Feb 22–23	Long Beach	USA
2	1989	Mar 13–14	Edinburgh	UK
3	1990	Mar 5–7	San Diego	USA
4	1991	Mar 18–10	Kyoto	Japan
5	1992	Mar 16–19	San Diego	USA
6	1993	Mar 22–25	Barcelona	Spain
7	1994	Mar 21–24	San Diego	USA
8	1995	Mar 22–25	Nara	Japan
9	1996	Mar 25–28	Trento	Italy
10	1997	Mar 17–20	Monterey	USA
11	1998	Mar 23–26	Kanazawa	Japan
12	1999	Mar 15–18	Göteborg	Sweden
13	2000	Mar 13–16	Monterey	USA
14	2001	Mar 19–22	Kobe	Japan
15	2002	Apr 8–11	Cork	Ireland
16	2003	Mar 17–20	Monterey	USA
17	2004	Mar 22–25	Awaji	Japan
18	2005	Apr 4–7	Leuven	Belgium
19	2006	Mar 6–9	Austin	USA
20	2007	Mar 19–22	Tokyo	Japan
21	2008	Mar 24–17	Edinburgh	UK
22	2009	Mar 30–Apr 1	Oxnard	USA
23	2010	Mar 22–25	Hiroshima	Japan
24	2011	Apr 04–07	Amsterdam	Netherlands
25	2012	Mar 19–22	San Diego	USA
26	2013	Mar 26–28	Osaka	Japan
27	2014	Mar 25–27	Udine	Italy
28	2015	Mar 24–26	Phoenix	USA
29	2016	Mar 29–31	Yokohama	Japan
30	2017	Mar 28–30	Grenoble	France
31	2018	Mar 20–22	Austin	USA
32	2019	Mar 19–21	Kita-Kyushu	Japan
33	**2020**	**Apr 6–9**	**Edinburgh**	**Scotland**